Tasmai D Joshi

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OBJECTIVE

Secure a responsible career opportunity to fully utilize my skills, while making a significant contribution to the success of the company. A technology enthusiast, finding opportunity to learn and explore new things and also to develop the required skill sets for future endeavors.

PROFESSIONAL TRAINING

Advanced VLSI Design and Verification course
Maven Silicon VLSI Design and Training Center, Bangalore
November 2019 till present.

EDUCATION QUALIFICATION

S. No.	Education	School/College	Marks (in %)
01	B.E.(EIE)	Bangalore Institute of Technology (VTU)	7.02 CGPA
02	Intermediate	K.L. E- S.Nijjalingappa PU College, Bangalore	85.83
03	X Std (ICSE)	S. Cadambi Vidya Kendra English Secondary School	84.16

SKILLS & ABILITIES

VLSI Domain Skills

HDL	:	Verilog
HVL	:	System Verilog
Verification Methodology	:	Coverage Driven Verification, Assertion Based Verification
TB Methodology	:	UVM
EDA Tools	:	QuestaSim- Mentor Graphics ISE-Xilinx
Domain	:	ASIC/FPGA front-end Design and Verification
Knowledge	:	RTL Coding, FSM based design, Simulation, Code Coverage, Functional Coverage, Static Timing Analysis, SVA.

Other Skills:

Language	:	OOP using C++, C programming.

CURRICULUM PROJECT	**1. Router 1x3 – RTL design and Verification** HDL: Verilog HVL: System Verilog TB Methodology: UVM EDA Tools: Questasim and ISE **Description:** The router accepts data packets on a single 8-bit port and routes them to one of the three output channels, channel0, channel1 and channel2. **Responsibilities:** ➢ Architected the block level structure for the design ➢ Implemented RTL using Verilog HDL ➢ Architected the class-based verification environment using System Verilog ➢ Verified the RTL model using System Verilog. ➢ Generated functional and code coverage for the RTL verification sign-off ➢ Synthesized the design. **2. UART-IP Core- Verification** HVL: SystemVerilog TB Methodology: UVM EDA Tools: Questasim **Description:** The UART IP core provides serial communication capabilities, which allow communication with modem or other external devices. UART will operate in three different modes – Simplex mode, Full Duplex mode and loopback mode. **Responsibilities:** ➢ Architected the class based verification environment in UVM ➢ Defined Verification Plan ➢ Verified the RTL module using SystemVerilog ➢ Generated functional and code coverage for the RTL verification sign-off
ACADEMIC PROJECTS	**Integrated Security Systems for SAS (Security Assurance Standards)** The project is based on integrating different security modules on a single platform. The security modules which were integrated are Door Access Control System (DACS), Surveillance System and Vehicle Access Control System (VACS). All these stand-alone systems were integrated on a single platform namely NIAGARA Framework which is an open source JAVA based framework.
INTERNSHIP	**Process Automation Intern at Cimtrix Systems** • Learned about basic operations of electrical components • Learned about PLC ladder logic • VFD (Variable Frequency Drive) operations • Basic operations of Servo Drive and Servo Motor

STRENGTHS	• Patience. • Curious to learn. • Quick learner.
PERSONAL DETAILS	Gender: Male Father's Name: D. M. Joshi Mother's Name: Nalini. D. Joshi Date of Birth: 16/10/1996 Languages Known: English, Hindi, Kannada, Telugu.
DECLERATION	I hereby declare that the information furnished above is true to the best of my knowledge. Date: Place: Bangalore (Tasmai D Joshi)