

MISC

FPGA

MEMORY

POL

JP4

1

2

3

4

5

6

7

8

9

10

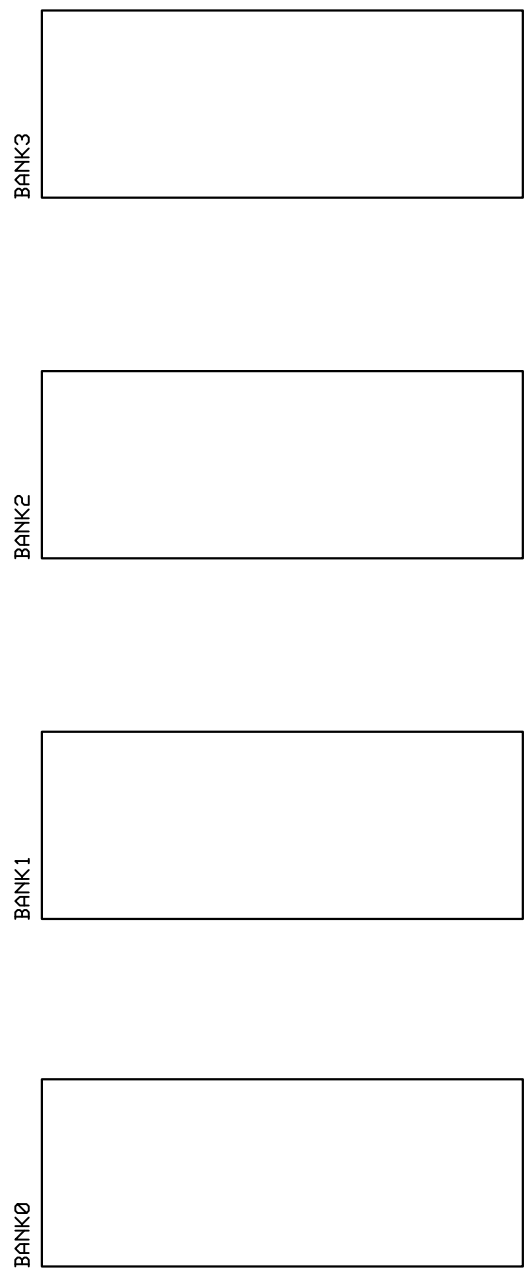
3V3 1V5 1V5A

3V3

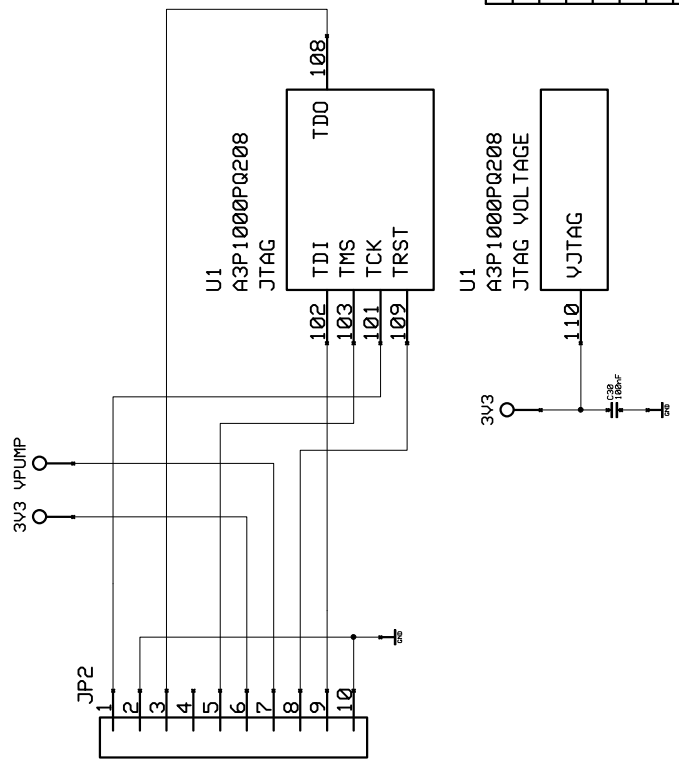
BT1638C-4

ORSoc

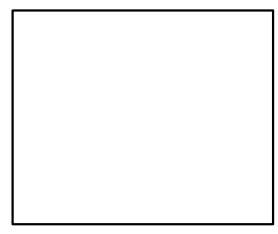
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Drawn	TOP	Release ECO	Release date
Checked		Replaces	02/11/09
		Drawing no.	Design rev.
			Page



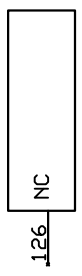
# JTAG config



FPGAPWR

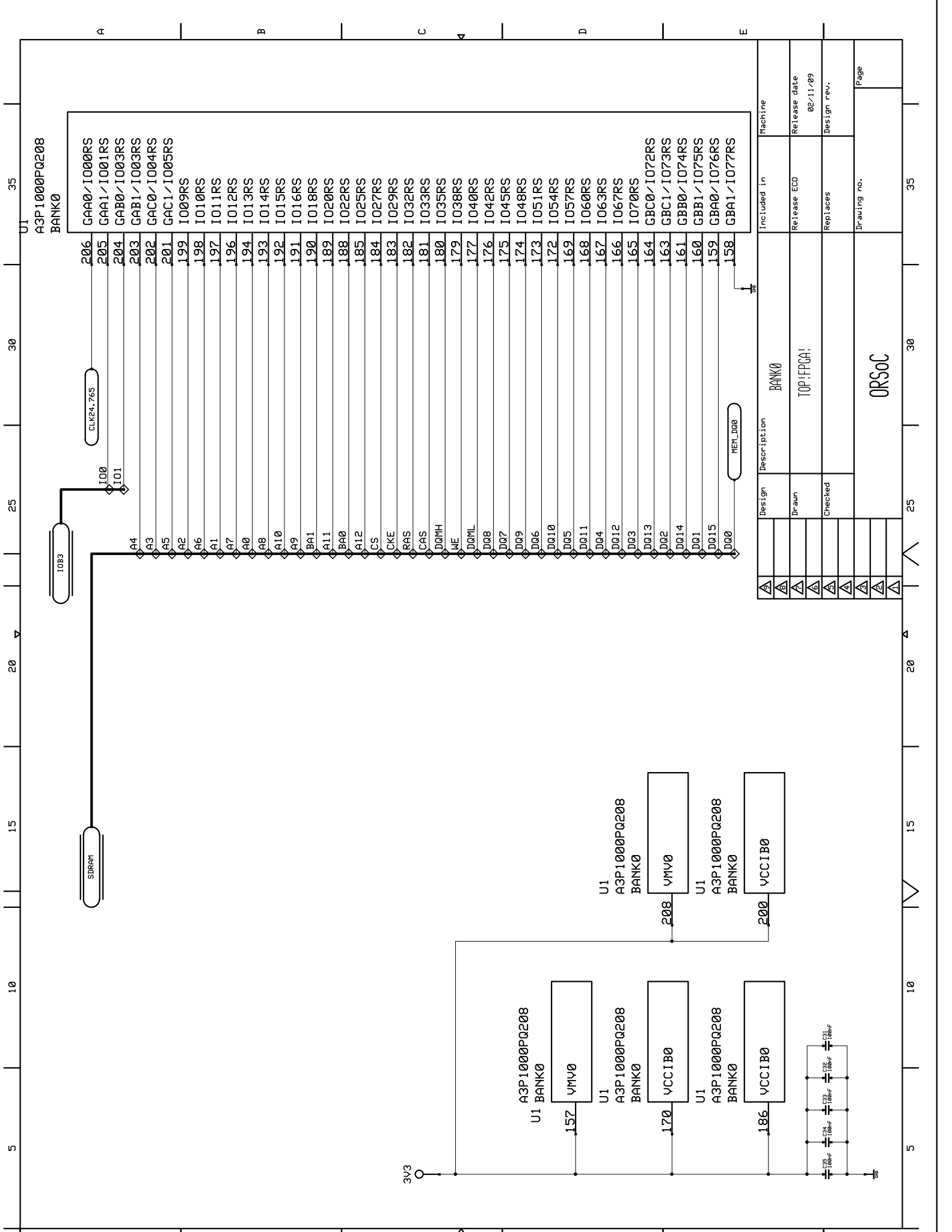


U1  
A3P1000PQ208  
NC



Design	Description	Included in	Machine
Drawn	FPGA	Release ECO	Release date
Checked	TOP!	Replaces	02/11/09
		Drawing no.	Design rev.
			Page

ORSoc



A3P1000PQ208 BANK0

206	GAA0/I000RS
205	GAA1/I001RS
204	GAB0/I003RS
203	GAB1/I003RS
202	GAC0/I004RS
201	GAC1/I005RS
199	I009RS
198	I010RS
197	I011RS
196	I012RS
194	I013RS
193	I014RS
192	I015RS
191	I016RS
190	I018RS
189	I020RS
188	I022RS
185	I025RS
184	I027RS
183	I029RS
182	I032RS
181	I033RS
180	I035RS
179	I038RS
177	I040RS
176	I042RS
175	I045RS
174	I048RS
173	I051RS
172	I054RS
169	I057RS
168	I060RS
167	I063RS
166	I067RS
165	I070RS
164	GBC0/I072RS
163	GBC1/I073RS
161	GBB0/I074RS
160	GBB1/I075RS
159	GBA0/I076RS
158	GBA1/I077RS

Design		Included in	Machine
Drawn	BANK0	Release ECO	Release date
Checked	TOP:FPGA1	Replaces	02/11/09
		Replaces	Design rev.
		Drawing no.	Page
			35

OR50C

3V3

A3P1000PQ208  
U1 BANK0

157 VMV0

A3P1000PQ208  
U1 BANK0

170 VCC1B0

A3P1000PQ208  
U1 BANK0

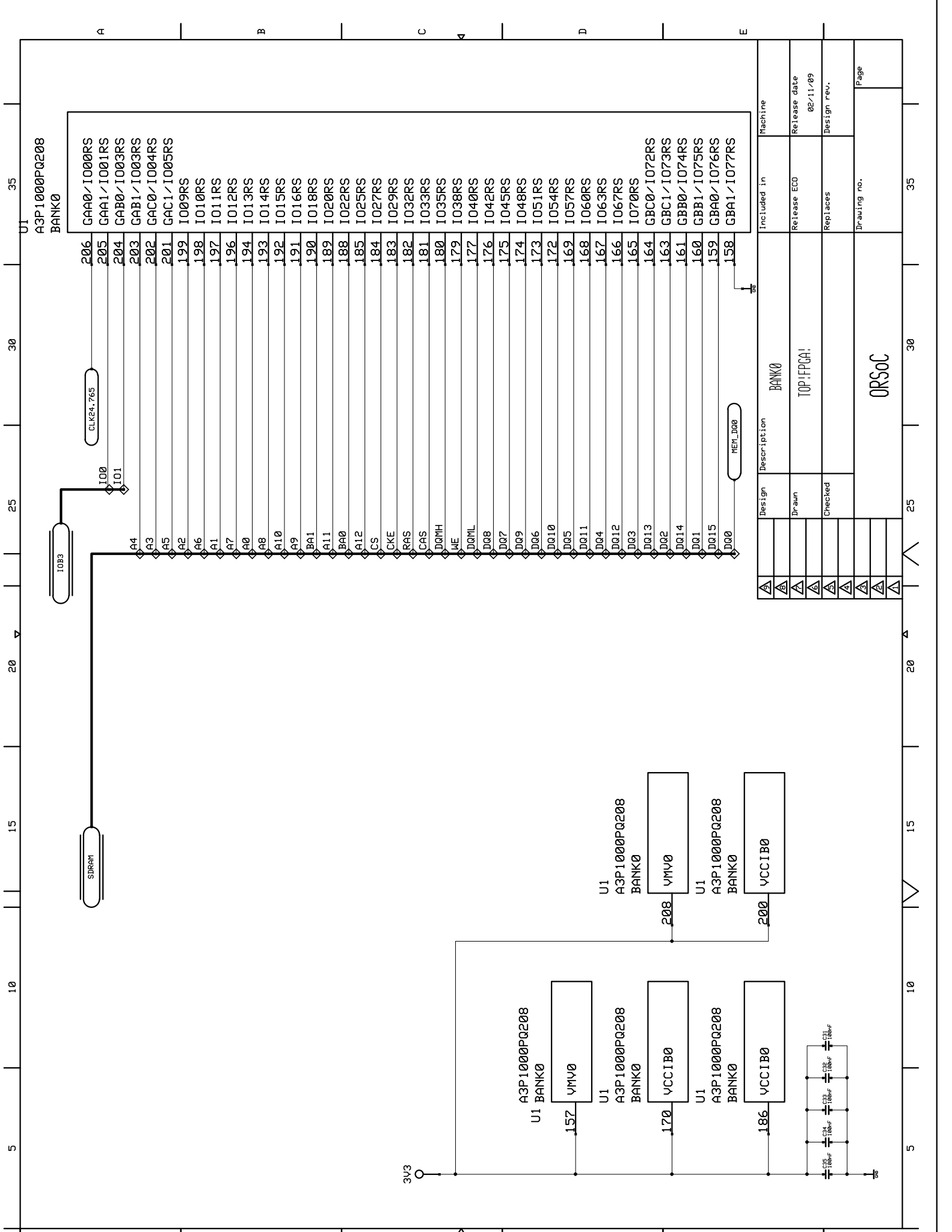
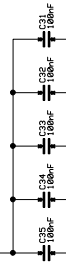
186 VCC1B0

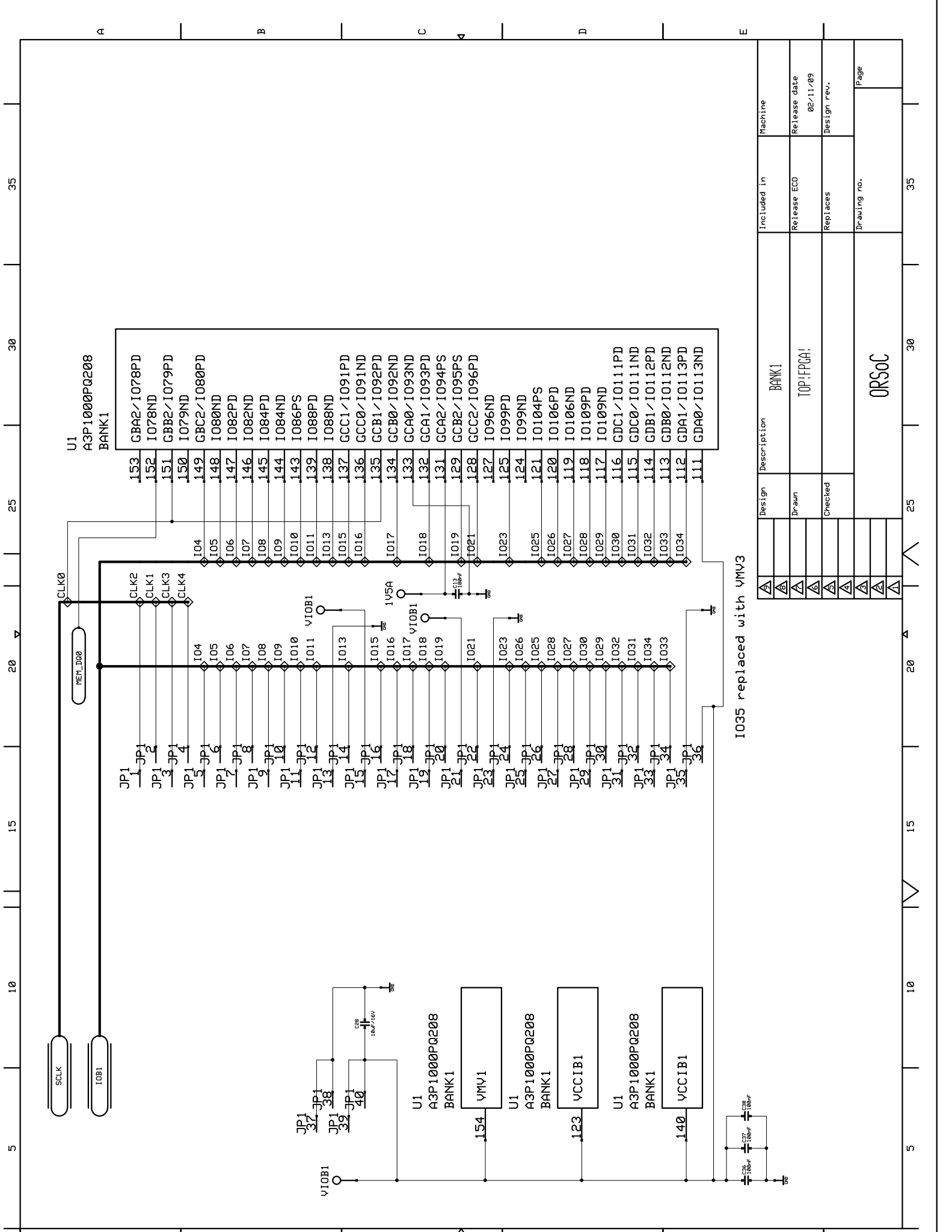
U1  
A3P1000PQ208  
BANK0

208 VMV0

U1  
A3P1000PQ208  
BANK0

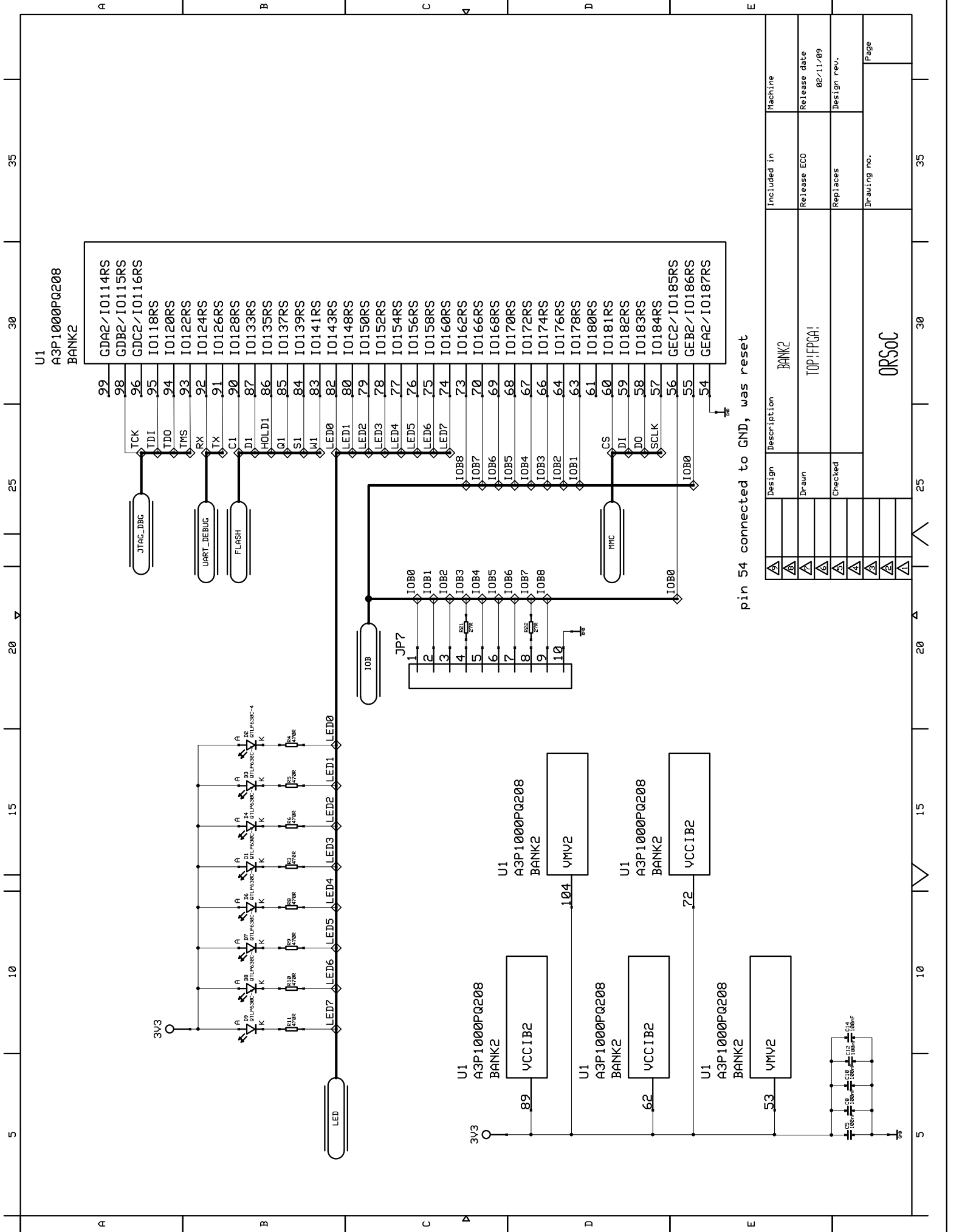
200 VCC1B0





I035 replaced with VMV3

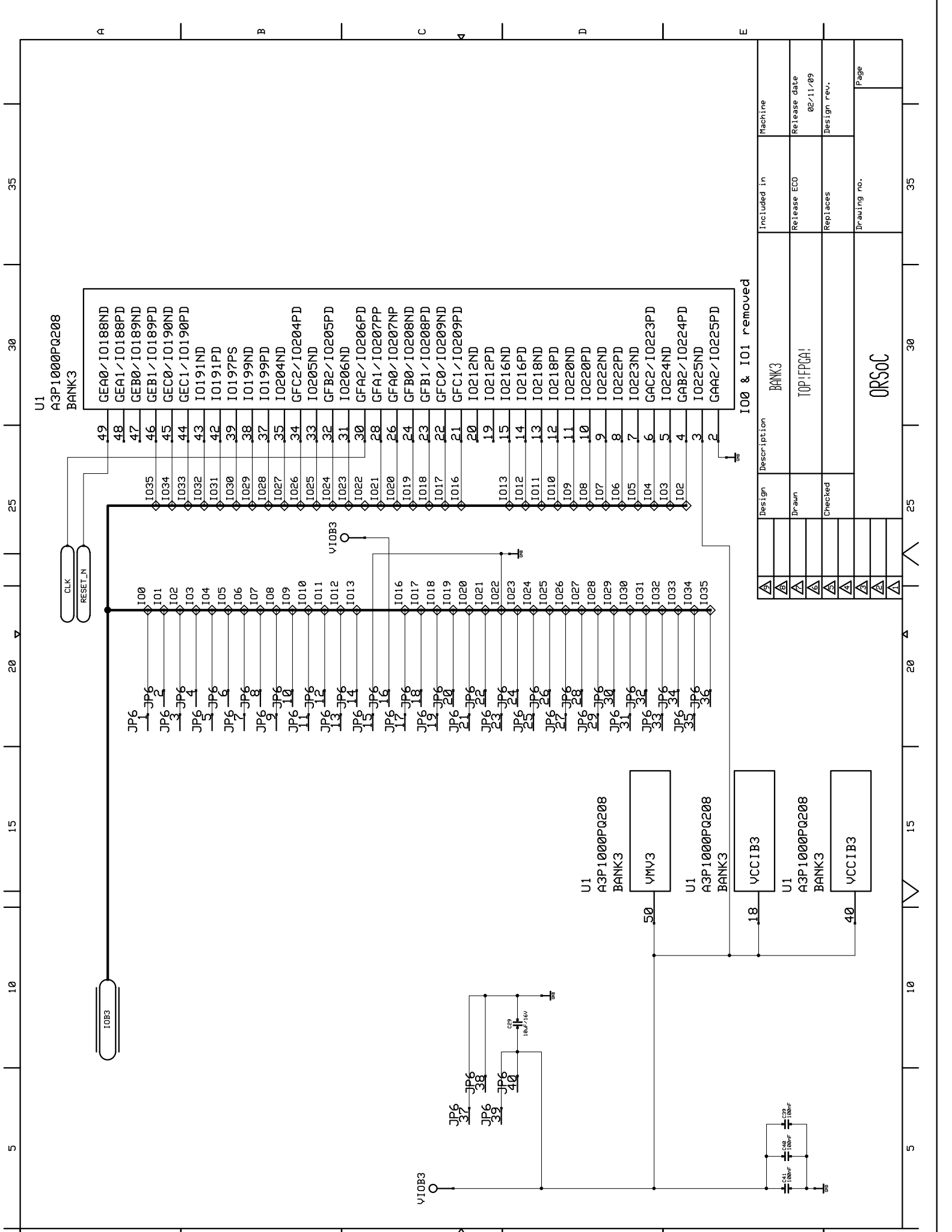
Design	Description	Included in	Machine
▲	BANK1	Release ECO	Release date
▲	TOP;FPGA;	Replaces	02/11/09
▲		Drawing no.	Design rev.
▲	OR50C		Page



pin 54 connected to GND, was reset

Design	Description	Included in	Machine
▲	BANK2	Release ECO	Release date
▲	TOP;FPGA;	Replaces	02/11/09
▲		Drawing no.	Design rev.
▲			Page

ORSOc



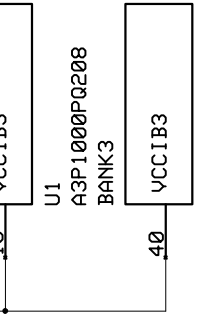
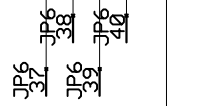
U1  
A3P1000PQ208  
BANK3

49	GEA0/I0188ND
48	GEA1/I0188PD
47	GEB0/I0189ND
46	GEB1/I0189PD
45	GEC0/I0190ND
44	GEC1/I0190PD
43	I0191ND
42	I0191PD
39	I0197PS
38	I0199ND
37	I0199PD
35	I0204ND
34	GFC2/I0204PD
33	I0205ND
32	GFB2/I0205PD
31	I0206ND
30	GFA2/I0206PD
28	GFA1/I0207PP
26	GFA0/I0207NP
24	GFB0/I0208ND
23	GFB1/I0208PD
22	GFC0/I0209ND
21	GFC1/I0209PD
20	I0212ND
19	I0212PD
15	I0216ND
14	I0216PD
13	I0218ND
12	I0218PD
11	I0220ND
10	I0220PD
9	I0222ND
8	I0222PD
7	I0223ND
6	GAC2/I0223PD
5	I0224ND
4	GAB2/I0224PD
3	I0225ND
2	GAA2/I0225PD

I00 & I01 removed

Design	Description	Included in	Machine
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△	TOP: FPGA;	Replaces	Design rev.
△		Drawing no.	Page

V10B3



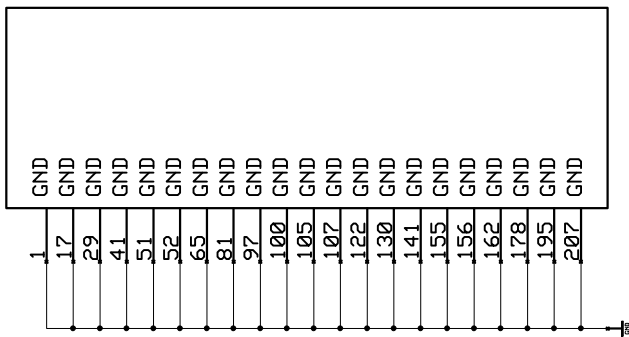
5 10 15 20 25 30 35

A B C D E

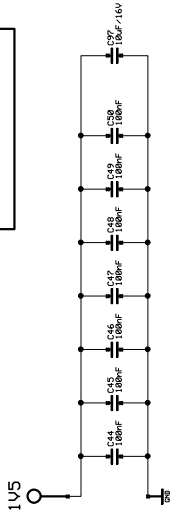
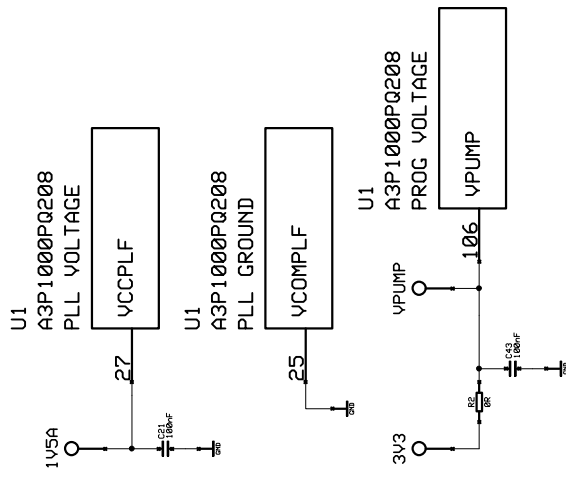
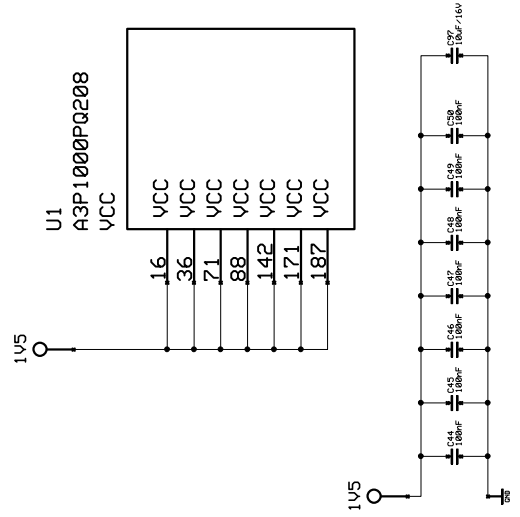
5 10 15 20 25 30 35

A B C D E

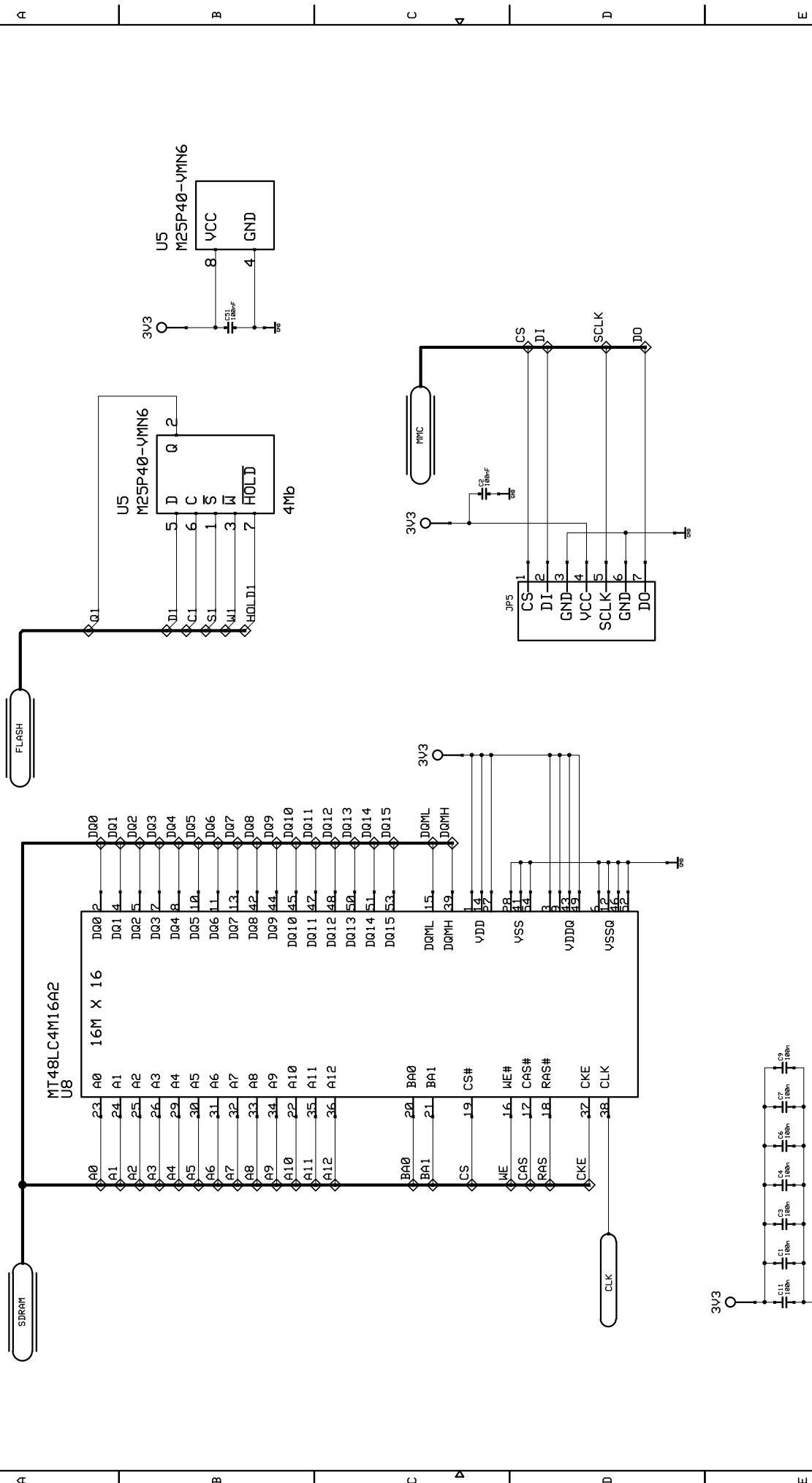
U1  
A3P1000PQ208  
GND



U1  
A3P1000PQ208  
VCC



Design	Description	Included in	Machine
	FPGA/MR		
	TOP;FPGA;	Release ECO	Release date 02/11/09
		Replaces	Design rev.
		Drawing no.	Page
OR50C			



Design	Description	Included in	Machine
Drawn	MEMORY	Release ECO	Release date
Checked	TOP!	Replaces	02/11/09
		Drawing no.	Design rev.
			Page

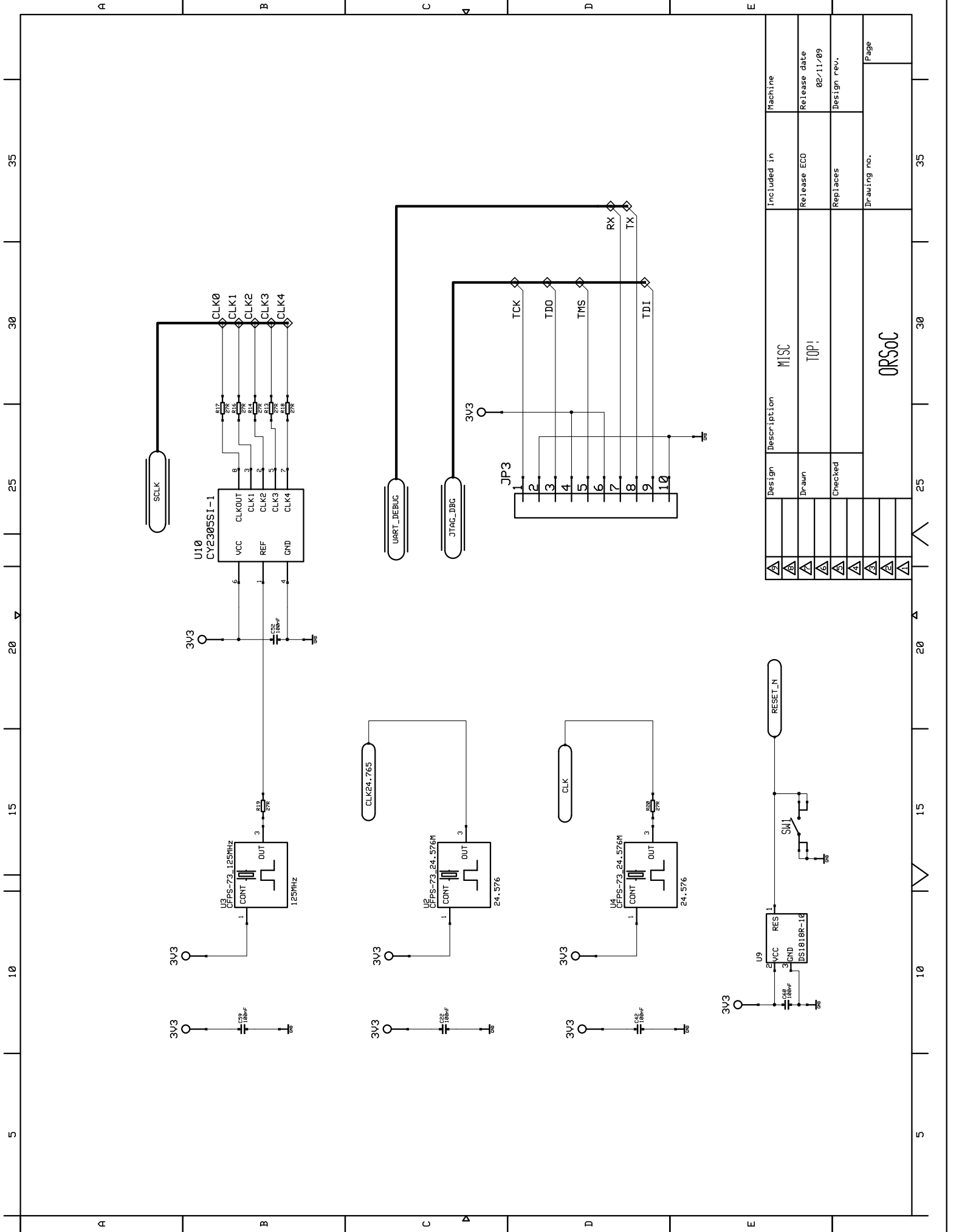
5 10 15 20 25 30 35

A B C D E

5 10 15 20 25 30 35

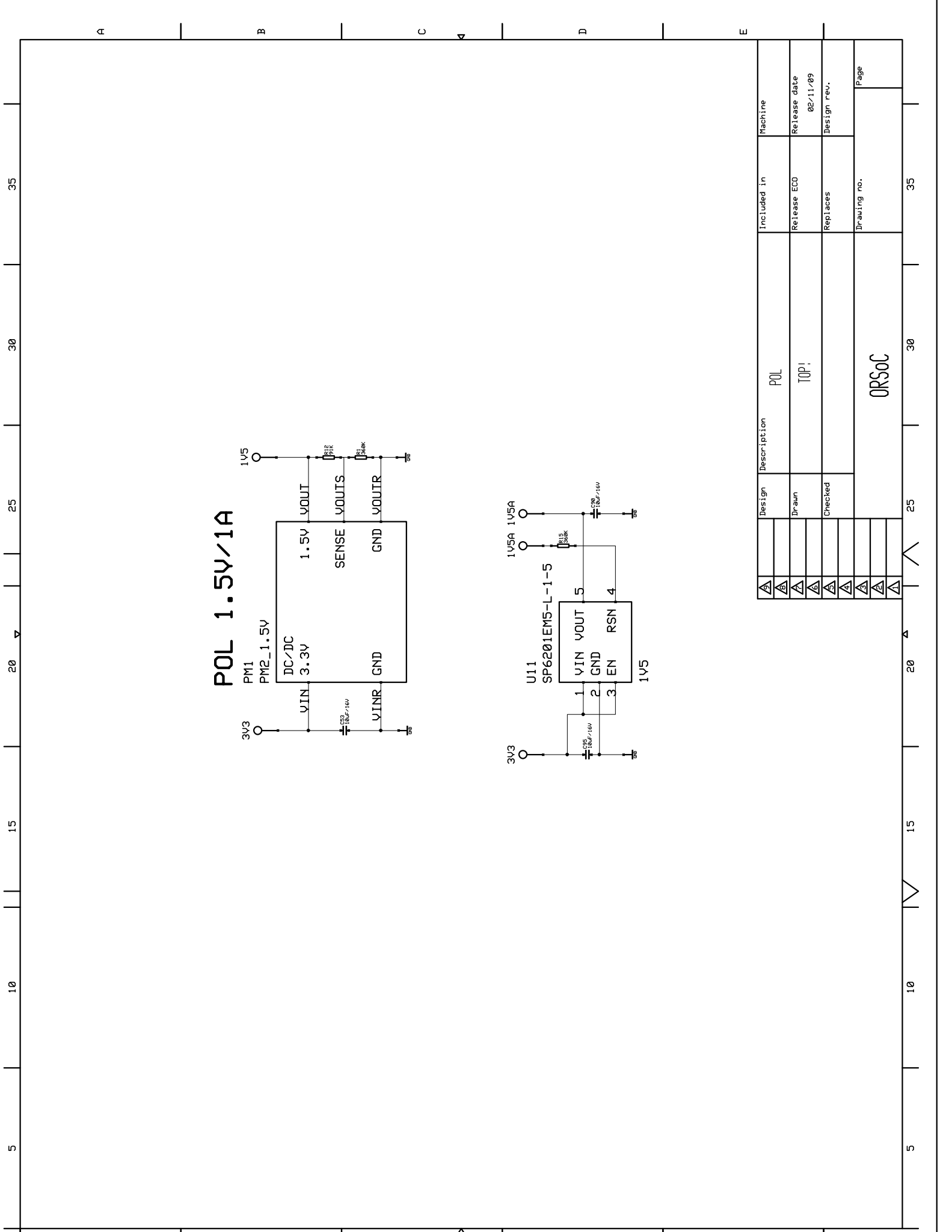
ORSoc



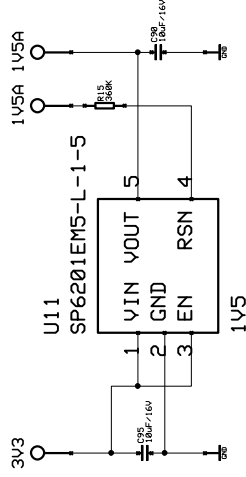
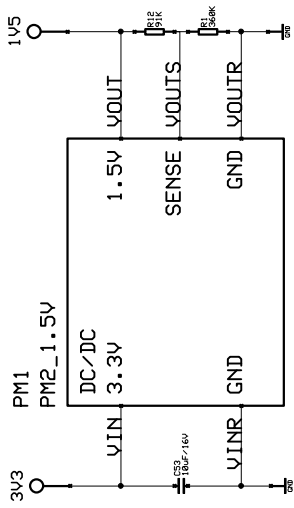


Design	Description	Included in	Machine
Drawn	MISC	Release ECO	Release date
Checked	TOP!	Replaces	02/11/09
		Drawing no.	Design rev.
			Page

ORSoC



# POL 1.5V/1A



Design	Description	Included in	Machine
Drawn	POL	Release ECO	Release date
Checked	TOP!	Replaces	02/11/09
		Drawing no.	Design rev.
			Page

ORSoC

